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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,780	05/11/2005	Matthias Brunner	ZIMR/0014	3146
7590	11/16/2006		EXAMINER	
Moser Patterson & Sheridan Zimmermann & Partner Suite 1500 3040 Post Oak Boulevard Houston, TX 77056			VELEZ, ROBERTO	
			ART UNIT	PAPER NUMBER
			2829	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/518,780	BRUNNER, MATTHIAS
	Examiner	Art Unit
	Roberto Velez	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 01 September 2006.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 30-58 is/are pending in the application.
- 4a) Of the above claim(s) 33-36,38,46 and 47 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 30-32,37,39-45 and 48-58 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 01 September 2006 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>12/04, 03/05, 05/05</u> .	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species of Fig. 3 in the reply filed on 09/01/2006 is acknowledged. The traversal is on the ground(s) that claims 33-36, 46 and 47 contain limitations necessarily searched with the examination of the remaining Claims in the application. Therefore, no serious burden is placed upon the Examiner to examine claims 33-36, 46 and 47. This is not found persuasive because claims 33-36, 46 and 47 reads on different Species (Figures 1 and 2) and require further search in different areas, for example class 349 and 345 that are related to liquid crystal display. Therefore, the Examiner will have a burden of searching in different classes for the difference apparatus features described in Figures 1-2.
2. The Examiner has withdrawn claim 38 since it reads on Non-Elected Species of Figure 2.
3. The requirement is still deemed proper and is therefore made FINAL.

Information Disclosure Statement

4. The Information Disclosure Statement (IDS) filed on 12/17/2004, 03/17/2005 and 05/16/2005 have been considered. However, based on the extensive number and the length of references cited, a cursory review was made. Applicant is advised to provide which of the cited references and/or contents thereof are most pertinent to the instant application, if a detailed consideration is desired.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 30-31, 37, 39-40, 49, 56-57 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Jenkins et al. (US Pat. 6,437,596)***.

Regarding claim 30, ***Jenkins et al.*** shows (Figures 1A-7) integrated circuits for testing a display array comprising: the drive circuit [19] has input terminals (where [23, 29] are connected) and output terminals (where [18] are connected); a first arrangement of contact areas [29] connected with the input terminals of the drive circuit [19]; and a second arrangement of contact areas [23] connected with the input terminals of the drive circuit [19] directly or via another component, wherein the contact areas [23] of the second arrangement of contact areas are larger (in size as shown in Fig. 1A) than the contact areas [29] of the first arrangement of contact areas.

Regarding claim 31, ***Jenkins et al.*** discloses everything as claimed above in claim 30; in addition, ***Jenkins et al.*** shows (Figures 1A-7) wherein the number of input terminals of the drive circuit [19] by which the drive circuit is connected with the second arrangement of contact areas [23] is at most 5% of the number of output terminals of the drive circuit [19] by which the drive circuit is connected with the control lines [18] of the matrix of picture elements [12].

Regarding claim 37, *Jenkins et al.* discloses everything as claimed above in claim 30; in addition, *Jenkins et al.* shows (Figures 1A-7) wherein the second arrangement of contact areas [23] is directly connected with the drive circuit [19].

Regarding claim 39, *Jenkins et al.* discloses everything as claimed above in claim 30; in addition, *Jenkins et al.* shows (Figures 1A-7) wherein the number of second pads of the second arrangement of contact areas [23] is at most 90% of the number of first pads of the first arrangement of contact areas [29].

Regarding claim 40, *Jenkins et al.* discloses everything as claimed above in claim 30; in addition, *Jenkins et al.* shows (Figures 1A-7) wherein the second pads of the second arrangement of contact areas [23] are larger than the first pads of the first arrangement of contact areas [29].

Regarding claim 49, *Jenkins et al.* discloses everything as claimed above in claim 30; in addition, *Jenkins et al.* shows (Figures 1A-7) a matrix of picture elements [12]; and drive electronics [19].

Regarding claim 56, *Jenkins et al.* shows (Figures 1A-7) integrated circuits for testing a display array comprising: providing a drive circuit [19]; connecting control lines [18] of the matrix of picture elements [12] with output terminals of the drive circuit [19]; providing a first arrangement of contact areas [29]; connecting the first arrangement of contact areas [29] with input terminals of the drive circuit [19]; providing a second arrangement of contact areas [23], said second arrangement of contact areas [23] being larger than the contact areas of said first arrangement of contact areas [29]; and connecting the second

arrangement of contact areas [23] with input terminals of the drive circuit [19] directly or via another component.

Regarding claim 57, *Jenkins et al.* discloses everything as claimed above in claim 30; in addition, *Jenkins et al.* shows (Figures 1A-7) An optoelectronic device [10, 12], which has been tested by a testing method according to claim 24 50 or by an apparatus according to claim 30.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 32, 41-45, 48, 50-52, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Jenkins et al.* (US Pat. 6,437,596) in view of *Matsuoka et al.* (US Pat. 6,188,453).

Regarding claim 32, *Jenkins et al.* discloses everything as claimed above in claim 30.

Jenkins et al. fails to disclose wherein the first arrangement of contact areas serves for picture generation during normal operation; and the second arrangement of contact areas serves for pattern generation during test mode. However, *Matsuoka et al.* discloses (Col 3, Ln 24-37) wherein the first arrangement of contact areas [8] serves for picture generation during normal

operation; and the second arrangement of contact areas [9] serves for pattern generation during test mode.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of *Matsuoka et al.* into the device of *Jenkins et al.* by providing first arrangement of contact areas for picture generation and second arrangement of contact areas for testing. The ordinary artisan would have been motivated to modify *Jenkins et al.* in the manner set forth above for the purpose of being able to use the device and test it simultaneously for the purpose of saving time.

Regarding claim 41, the combination of *Jenkins et al.* and *Matsuoka et al.* discloses everything as claimed above in claim 30.

The combination of *Jenkins et al.* and *Matsuoka et al.* is silent about disclosing second pads of the second arrangement of contact areas having a dimension of at least 100 μm .

It would have been an obvious matter of design choice to have second pads of the second arrangement of contact areas with a dimension of at least 100 μm , since applicant has not disclosed that second pads of the second arrangement of contact areas having a dimension of at least 100 μm solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with any size of pads as long as the probes are able to make contact with the pad are to run a test.

Regarding claim 42, *Jenkins et al.* shows (Figures 1A-7) integrated circuits for testing a display array comprising: at least one pad [29]; at least one connection of the at least one pad [29] with a drive circuit [19] directly or via another component, wherein the arrangement of test contact areas [23] are larger (in size as shown in Fig. 1A) than the arrangement of operational contact areas [29].

Jenkins et al. fails to disclose at least one pad is provided with signals via an arrangement of operational contact areas during normal operation. However, *Matsuoka et al.* discloses (Col 3, Ln 24-37) wherein the at least one pad [8] is provided with signals via an arrangement of operational contact areas during normal operation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of *Matsuoka et al.* into the device of *Jenkins et al.* by providing at least one pad with signals via an arrangement of operational contact areas during normal operation. The ordinary artisan would have been motivated to modify *Jenkins et al.* in the manner set forth above for the purpose of being able to use the device and test it simultaneously for the purpose of saving time.

Regarding claim 43, the combination of *Jenkins et al.* and *Matsuoka et al.* discloses everything as claimed above in claim 42; in addition, *Jenkins et al.* shows (Fig. 1A) the drive circuit [19] has input terminals and output terminals,

and wherein the at least one connection [29] is connected with at least one of the input terminals.

Regarding claim 44, the arguments used for the rejection of claim 41 regarding this feature, also apply.

Regarding claim 45, the arguments used for the rejection of claim 39 regarding this feature, also apply.

Regarding claim 48, the combination of *Jenkins et al.* and *Matsuoka et al.* discloses everything as claimed above in claim 42; in addition, *Jenkins et al.* shows (Fig. 1A) wherein the arrangement of test contact areas [23] is directly connected with the drive circuit [19].

Regarding claim 50, *Jenkins et al.* shows (Figures 1A-7) integrated circuits for testing a display array comprising: making contact (using probes connected to [40]) between an external control [52, 46, 34] and an arrangement of test contact areas [23] which are larger (in size as shown in Fig. 1A) than other contact areas [29]; providing an input terminal of a drive circuit [19] directly or via another component with input signals via the arrangement of test contact areas [23] to generate a test pattern (using [52, 46, 34]) on a matrix of picture elements [10, 12]; and testing (using [52, 46, 34]) the picture elements [12] of the matrix of picture elements [10, 12].

Jenkins et al. fails to disclose an arrangement of operational contact areas. However, *Matsuoka et al.* discloses (Col 3, Ln 24-37) wherein arrangement of operational contact areas [8].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of *Matsuoka et al.* into the device of *Jenkins et al.* by providing arrangement of operational contact areas. The ordinary artisan would have been motivated to modify *Jenkins et al.* in the manner set forth above for the purpose of being able to use the device and test it simultaneously for the purpose of saving time.

Regarding claim 51, the combination of *Jenkins et al.* and *Matsuoka et al.* discloses everything as claimed above in claim 50; in addition, *Jenkins et al.* shows (Fig. 1A) wherein the input signals generate a periodic test pattern.

Regarding claim 52, the combination of *Jenkins et al.* and *Matsuoka et al.* discloses everything as claimed above in claim 50; in addition, *Jenkins et al.* shows (Fig. 1A) wherein the input signals generate a vertically, horizontally or diagonally periodic test pattern (depending which picture element is going to be tested).

Regarding claim 55, the combination of *Jenkins et al.* and *Matsuoka et al.* discloses everything as claimed above in claim 50; in addition, *Jenkins et al.* shows (Fig. 1A) wherein step c) comprises the following steps: the picture elements [12] in a portion of the matrix of picture elements [10, 12] are tested (using [52, 46, 34]); the optoelectronic device [10, 12] is shifted (using switches as shown in Fig. 3); and the picture elements [12] in a further portion of the matrix of picture elements [10, 12] are tested (using [52, 46, 34]).

9. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Jenkins et al. (US Pat. 6,437,596)** and **Matsuoka et al. (US Pat. 6,188,453)** as applied to claim 50, and further in view of **Henley (US Pat. 5,432,461)**.

Regarding claim 53, the combination of **Jenkins et al.** and **Matsuoka et al.** discloses everything as claimed above in claim 50.

The combination of **Jenkins et al.** and **Matsuoka et al.** fails to disclose wherein the picture elements are tested with a beam of charged particles or laser radiation. However, **Henley** shows (Fig. 1) wherein the picture elements are tested with a beam of charged particles or laser radiation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of **Henley** into the device of the combination of **Jenkins et al.** and **Matsuoka et al.** by testing the picture elements with a beam of charged particles or laser radiation. The ordinary artisan would have been motivated to modify the combination of **Jenkins et al.** and **Matsuoka et al.** in the manner set forth above for the purpose of testing the picture elements without using mechanical contact in order to avoid material corrosion.

10. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Jenkins et al. (US Pat. 6,437,596)** and **Matsuoka et al. (US Pat. 6,188,453)** as applied to claim 50, and further in view of **Kim (US Pat. 6,486,927)**.

Regarding claim 54, the combination of **Jenkins et al.** and **Matsuoka et al.** discloses everything as claimed above in claim 50.

The combination of **Jenkins et al.** and **Matsuoka et al.** fails to disclose further comprising the step of: a vacuum is generated in the vicinity of the optoelectronic device to be tested. However, **Kim** discloses (Col 5, Ln 43-48) wherein a vacuum is generated in the vicinity of the optoelectronic device to be tested.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of **Kim** into the device of the combination of **Jenkins et al.** and **Matsuoka et al.** by providing a vacuum is generated in the vicinity of the optoelectronic device to be tested. The ordinary artisan would have been motivated to modify the combination of **Jenkins et al.** and **Matsuoka et al.** in the manner set forth above for the purpose of attaching and securing the optoelectronic device to a stage while testing it.

11. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Jenkins et al. (US Pat. 6,437,596)** in view of **Tomita (US Pat. 6,924,875)**.

Regarding claim 58, **Jenkins et al.** discloses everything as claimed above in claims 30 and 49.

Jenkins et al. fails to disclose wherein at least parts of the second arrangement of contact areas are removed. However, **Tomita** shows (Fig. 1) wherein at least parts of the second arrangement of contact areas are removed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of **Tomita** into the device of **Jenkins et al.** by at least removing parts of the second arrangement of contact areas. The ordinary artisan would have been motivated to modify **Jenkins et al.** in the manner set forth above for the purpose of saving space in order to being able to add more picture elements.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Ha can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

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RV

Roberto Velez
Patent Examiner

Parish Patel
11/09/06
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PRIMARY EXAMINER